IN THE CLAIMS

Please amend claims 2, 3, and 5-8; cancel claims 1 and 4; and add claim 9-12 as follows:

1. (Canceled)

2. (Currently Amended) ~~The semiconductor memory device according to claim 1, wherein the control circuit further comprises another~~ A semiconductor memory device comprising:

an array of memory cells that is provided for memorizing data;

an address circuit responsive to an address signal inputted from an external source for addressing a memory cell in the array;

a write circuit responsive to a write signal inputted from an external source for writing the data into the addressed memory cell; and

a control circuit that is provided for delaying an input timing of the write signal to the write circuit by a given delay amount so as to adjust a timing of writing the data after addressing the memory cell, wherein

the control circuit comprises a first register capable of registering control data from an external source for setting the delay amount, a delay circuit for delaying the write signal by the set delay amount and outputting the delayed write signal to the write circuit, a second register capable of registering control data from an ~~outside~~ external source for determining an assertion duration of the write signal, and an assertion setting circuit for setting the assertion duration of the write signal according to the registered control data so that the write circuit is activated for writing the data during the set assertion duration.

3. (Currently Amended) ~~The semiconductor memory device according to claim 1,~~ A semiconductor memory device comprising:

an array of memory cells that is provided for memorizing data;

an address circuit responsive to an address signal inputted from an external source for addressing a memory cell in the array;

a write circuit responsive to a write signal inputted from an external source for writing the data into the addressed memory cell; and

a control circuit that is provided for delaying an input timing of the write signal to the write circuit by a given delay amount so as to adjust a timing of writing the data after addressing the memory cell, wherein

the control circuit includes a first register capable of registering control data from an external source for setting the delay amount, a delay circuit for delaying the write signal by the set delay amount and outputting the delayed write signal to the write circuit, and ~~wherein~~ the delay circuit ~~comprises~~ includes a plurality of delay lines, each delay line ~~comprising~~ including a different number of amplifiers connected in series to define a different delay amount, and a selector for selecting one of the delay lines according to the registered control data so that the selected delay line is used to delay the write signal.

4. (Canceled)

5. (Currently Amended) ~~The semiconductor memory device according to claim 4, wherein the control circuit further comprises another~~ A semiconductor memory device comprising:

an array of memory cells that memorizes data;

an address circuit responsive to an address signal inputted from an external source for addressing a memory cell in the array;

a read circuit responsive to a read signal inputted from an external source for reading the data from the addressed memory cell; and

a control circuit for delaying an input timing of the read signal to the read circuit by a

given delay amount so as to adjust a timing of reading the data after addressing the memory cell, wherein

the control circuit includes a register capable of registering control data from an external source for setting the delay amount, a delay circuit for delaying the read signal by the set delay amount and outputting the delayed read signal to the read circuit, and a second register capable of registering control data from an ~~outside~~ external source for determining an assertion duration of the read signal, and an assertion setting circuit for setting the assertion duration of the read signal according to the registered control data so that the read circuit is activated for reading the data during the set assertion duration.

6. (Currently Amended) ~~The semiconductor memory device according to claim 4, wherein the delay circuit comprises~~ A semiconductor memory device comprising:

an array of memory cells that memorizes data;

an address circuit responsive to an address signal inputted from an external source for addressing a memory cell in the array;

a read circuit responsive to a read signal inputted from an external source for reading the data from the addressed memory cell; and

a control circuit for delaying an input timing of the read signal to the read circuit by a given delay amount so as to adjust a timing of reading the data after addressing the memory cell, wherein

the control circuit includes a register capable of registering control data from an external source for setting the delay amount, and a delay circuit for delaying the read signal by the set delay amount and outputting the delayed read signal to the read circuit, the delay circuit

including a plurality of delay lines, each delay line comprising a different number of amplifiers connected in series to define a different delay amount, and a selector for selecting one of the delay lines according to the registered control data so that the selected delay line is used to delay the read signal.

7. (Currently Amended) ~~The semiconductor memory device according to claim 4, wherein the control circuit comprises~~ A semiconductor memory device comprising:

an array of memory cells that memorizes data;

an address circuit responsive to an address signal inputted from an external source for addressing a memory cell in the array;

a read circuit responsive to a read signal inputted from an external source for reading the data from the addressed memory cell; and

a control circuit for delaying an input timing of the read signal to the read circuit by a given delay amount so as to adjust a timing of reading the data after addressing the memory cell, wherein

the control circuit includes a register capable of registering control data from an external source for setting the delay amount, a delay circuit for delaying the read signal by the set delay amount and outputting the delayed read signal to the read circuit, and an OR gate circuit, an AND gate circuit and variable delay circuits including a first delay circuit, a second delay circuit and a third delay circuit, the first delay circuit initially delaying the read signal and outputting the initially delayed read signal as a word signal for the memory cell, the second delay circuit being connected in series to the first delay circuit for subsequently delaying the initially delayed read signal and outputting the subsequently delayed read signal, the OR gate circuit having an input

terminal for receiving the read signal, another input terminal for receiving the subsequently delayed read signal, and an output terminal for feeding an OR-gated read signal as a precharge signal to the memory cell, the AND gate circuit having an input terminal for receiving the read signal, another input terminal for receiving the subsequently delayed read signal and an output terminal for feeding an AND-gated read signal having a given assertion duration such that the AND gate circuit, the first delay circuit and the second delay circuit constitute an assertion setting circuit for setting the assertion duration of the read signal so that the read circuit is activated for reading the data during the assertion duration, the third delay circuit being connected to the output terminal of the AND gate circuit for finally delaying the AND-gated read signal by the set delay amount such that the third delay circuit constitutes the delay circuit for delaying the read signal by the set delay amount and outputting the finally delayed read signal to the read circuit.

8. (Currently Amended) A ~~control~~ method of a controlling semiconductor memory device having an array of memory cells for memorizing data, an address circuit responsive to an address signal inputted from an ~~outside~~ external source for addressing a memory cell in the array, and a write circuit responsive to a write signal inputted from an ~~outside~~ external source for writing the data into the addressed memory cell, the ~~control~~ method comprising ~~the steps of~~:

registering control data into an internal register from an ~~outside~~ external source for setting an optimal delay amount;

registering control data from an external source for determining an assertion duration of the write signal;

setting the assertion duration of the write signal according to the registered control data

so that the write circuit is activated for writing the data during the set assertion duration;

setting the optimal delay amount to an internal delay circuit according to the registered control data; and

outputting the write signal delayed by the set delay amount from the internal delay circuit to the write circuit so as to adjust a timing of writing the data after addressing the memory cell.

9. (New) A method of a controlling semiconductor memory device having an array of memory cells for memorizing data, an address circuit responsive to an address signal inputted from an external source for addressing a memory cell in the array, and a write circuit responsive to a write signal inputted from an external source for writing the data into the addressed memory cell, the control method comprising:

registering control data into an internal register from an external source for setting an optimal delay amount;

registering control data from an external source for determining an assertion duration of the write signal;

reading a read signal inputted from an external source for reading the data from the addressed memory cell;

setting the assertion duration of the write signal according to the registered control data so that the write circuit is activated for writing the data during the set assertion duration;

setting the optimal delay amount to an internal delay circuit according to the registered control data; and

outputting the write signal delayed by the set delay amount from the internal delay circuit to the write circuit so as to adjust a timing of writing the data after addressing the memory cell.

10. (New) The semiconductor memory device according to claim 2, wherein the delay circuit includes a plurality of delay lines, each delay line including a different number of amplifiers connected in series to define a different delay amount, and a selector for selecting one of the delay lines according to the registered control data so that the selected delay line is used to delay the write signal.

11. (New) The semiconductor memory device according to claim 5, wherein the delay circuit includes a plurality of delay lines, each delay line including a different number of amplifiers connected in series to define a different delay amount, and a selector for selecting one of the delay lines according to the registered control data so that the selected delay line is used to delay the read signal.

12. (New) The semiconductor memory device according to claim 5, wherein the control circuit includes an OR gate circuit, an AND gate circuit and variable delay circuits including a first delay circuit, a second delay circuit and a third delay circuit, the first delay circuit initially delaying the read signal and outputting the initially delayed read signal as a word signal for the memory cell, the second delay circuit being connected in series to the first delay circuit for subsequently delaying the initially delayed read signal and outputting the subsequently delayed read signal, the OR gate circuit having an input terminal for receiving the read signal, another input terminal for receiving the subsequently delayed read signal, and an output terminal for feeding an OR-gated read signal as a precharge signal to the memory cell, the AND gate circuit having an input terminal for receiving the read signal, another input terminal for receiving the subsequently delayed read signal and an output terminal for feeding an AND-gated read signal having a given assertion duration such that the AND gate circuit, the first delay circuit and the

second delay circuit constitute an assertion setting circuit for setting the assertion duration of the read signal so that the read circuit is activated for reading the data during the assertion duration, the third delay circuit being connected to the output terminal of the AND gate circuit for finally delaying the AND-gated read signal by the set delay amount such that the third delay circuit constitutes the delay circuit for delaying the read signal by the set delay amount and outputting the finally delayed read signal to the read circuit.

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